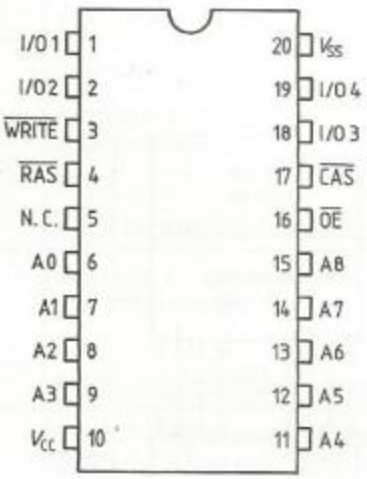
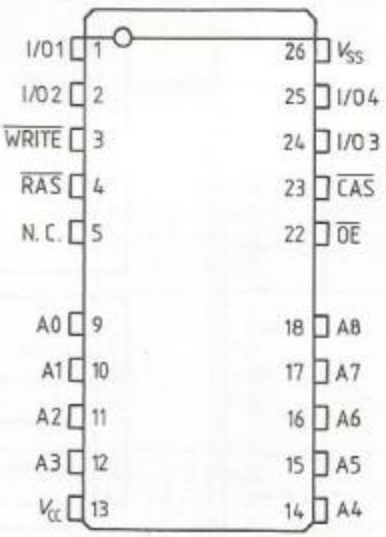
SIEMENS

HYB 514256-85/-10/-12
262144x4-Bit Dynamic RAM

- 262144 words by 4-bit organization
- Fast access and cycle time
  85 ns access time
  165 ns cycle time (HYB 514256-85)
  100 ns access time
  190 ns cycle time (HYB 514256-10)
  120 ns access time
  220 ns cycle time (HYB 514256-12)
- Fast page mode cycle time
  50 ns (HYB 514256-85)
  55 ns (HYB 514256-10)
  70 ns (HYB 514256-12)
- Single +5V (±10%) supply with a built-in V_{BB} generator
- Low power dissipation
  max. 413 mW active (HYB 514256-85)
  max. 358 mW active (HYB 514256-10)
  max. 303 mW active (HYB 514256-12)
  max. 5.5 mW standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, and fast page mode capability
- All inputs and outputs TTL-compatible
- 512 refresh cycles/8 ms
- Plastic Packages: P-DIP-20
  P-SOJ-26-20

Pin Configuration





The HYB 514256 is the new generation dynamic RAM organized as 262144 words by 4-bit. The HYB 514256 utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514256 to be packaged in a standard 20-pin or in a 26-20-pin (SOJ) plastic package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. Systemoriented features include single +5V (±10%) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.