

Contents

| SECTION | PAGE |
|--|------|
| 1. Introduction | 9 |
| 1.1 Purpose | 9 |
| 1.2 Scope | 9 |
| 2. Applicable Documents | 9 |
| 2.1 Industry Standards — American National Standards | 9 |
| 2.2 Military Standards | 10 |
| 2.3 International Standards | 10 |
| 3. Definitions | 11 |
| 4. General Requirements | 12 |
| 4.1 Content | 12 |
| 4.1.1 Basic Logic Diagram | 12 |
| 4.1.2 Detailed Logic Diagram | 12 |
| 4.1.3 Combined Forms of Circuit Diagrams | 13 |
| 4.2 Drawing Size and Format | 13 |
| 4.2.1 Drawing Zones | 13 |
| 4.2.2 Supplemental Drawing Number Location | 13 |
| 4.3 Diagram Titles | 13 |
| 4.4 Diagram Revisions | 13 |
| 4.5 Lettering | 13 |
| 4.6 Lines | 14 |
| 4.7 Abbreviations | 14 |
| 4.8 Letter Symbols | 14 |
| 4.9 Layout and Presentation | 15 |
| 4.9.1 Coverage | 15 |
| 4.9.2 Planning | 15 |
| 4.9.3 Signal Flow | 15 |
| 4.9.4 Layout | 15 |
| 4.9.5 Grouping of Symbols | 15 |
| 5. Logic Conventions and Polarity Indication | 16 |
| 5.1 Relationship Between Logic States and Logic Levels | 16 |
| 5.2 Single Logic Convention | 16 |
| 5.2.1 Positive Logic Convention | 16 |
| 5.2.2 Negative Logic Convention | 17 |
| 5.3 Direct Polarity Indication | 17 |
| 6. Symbols for Devices and Functions | 18 |
| 6.1 Standard Symbols | 18 |
| 6.1.1 Symbols for Logic Elements | 18 |
| 6.1.2 Distributed Connections (Dot-AND, Dot-OR) | 18 |
| 6.2 Size | 23 |
| 6.3 Orientation | 23 |
| 6.3.1 Orientation of Logic Symbol Lettering | 23 |
| 6.3.2 Orientation of Qualifying Symbols Derived from Characteristic Curves | 26 |
| 6.4 Application and Identification Information | 26 |
| 6.4.1 Types of Application Information | 26 |
| 6.4.1.1 Reference Designation | 26 |
| 6.4.1.2 Element Physical Identification | 27 |
| 6.4.1.3 Physical Location of Device | 27 |
| 6.4.1.4 Functional Use | 27 |
| 6.4.1.5 Terminal Identification | 27 |
| 6.4.1.6 Other Information | 27 |

| | | |
|-----------|--|----|
| 6.4.2 | Application Information Placement | 27 |
| 6.4.2.1 | Logic Symbols | 28 |
| 6.4.2.2 | Nonlogic Symbols | 28 |
| 6.5 | Inputs and Outputs with Multiple Functions | 29 |
| 6.6 | Abbreviated Representation of Symbols | 30 |
| 6.6.1 | Identical Inputs and Outputs | 30 |
| 6.6.2 | Arrays of Identical Elements | 30 |
| 6.7 | Abutment of Symbols | 32 |
| 6.8 | Detached Representation of Symbols | 32 |
| 6.9 | Unused Terminals and Elements | 33 |
| 6.10 | Devices Having a Large Number of Terminals | 33 |
| 7. | Interconnection of Symbols | 34 |
| 7.1 | General Requirements | 34 |
| 7.2 | Line Spacing | 34 |
| 7.3 | Junctions and Crossovers | 34 |
| 7.4 | Interrupted Lines | 35 |
| 7.5 | Grouping of Lines | 36 |
| 7.6 | Polarity and Negation Matching | 36 |
| 7.7 | Power Connections | 37 |
| 8. | Labeling of Connecting Lines | 37 |
| 8.1 | General | 37 |
| 8.2 | Names for Logic and Analog Signals | 38 |
| 8.2.1 | General Requirements | 38 |
| 8.2.1.1 | Descriptive Requirements | 38 |
| 8.2.1.2 | Recommended Characters | 38 |
| 8.2.1.3 | Length | 38 |
| 8.2.1.4 | Similar and Equivalent Signals | 38 |
| 8.2.2 | Binary Logic Signals | 40 |
| 8.2.2.1 | Signal State | 40 |
| 8.2.2.1.1 | Negated Signals | 41 |
| 8.2.2.1.2 | Arithmetic and Logical Expressions | 41 |
| 8.2.2.1.3 | Bus Signals and Other Grouped Signals | 42 |
| 8.2.2.1.4 | Clock Signals | 42 |
| 8.2.2.2 | Signal Level | 42 |
| 8.2.3 | Analog Signals | 45 |
| 8.3 | Names for Power and Other Constant-Level Connections | 45 |
| 8.4 | Locator Information | 45 |
| 8.4.1 | Cross-Reference Information | 45 |
| 8.4.2 | Physical Access Information | 45 |
| 8.5 | Additional Properties and Characterization | 45 |
| 9. | Supplementary Information | 46 |
| 9.1 | Reference-Designation Accounting | 46 |
| 9.2 | Diagram Notes | 46 |
| 9.2.1 | General Notes | 46 |
| 9.2.2 | Local Notes | 46 |
| 9.2.3 | Referenced (Indexed) Notes | 47 |
| 9.2.4 | Examples | 47 |
| 9.3 | Tabular Information | 47 |
| 9.4 | Waveforms | 48 |
| 9.4.1 | Use | 48 |
| 9.4.2 | Stylized Waveforms | 48 |
| 9.4.3 | Simplified Waveform Notations | 49 |

| | | |
|-------|--|----|
| 9.5 | Diagram Simplification and Abbreviation Techniques | 50 |
| 9.5.1 | Repeated Symbol Simplification | 50 |
| 9.5.2 | Repeated Circuit Patterns | 51 |
| 9.5.3 | Connections Paired with Ground | 54 |
| 9.5.4 | Circuit Layout Condensation | 55 |
| 10. | Examples of Logic Diagrams | 58 |

FIGURES

| | | |
|--------|---|----|
| Fig 1 | Line Conventions for Diagrams | 14 |
| Fig 2 | Distributed Connections | 20 |
| Fig 3 | Distributed Connections with a Mix of Negated and Unnegated Outputs (Positive Logic Shown) | 22 |
| Fig 4 | Distributed Connections with a Mix of Active-High and Active-Low Outputs | 22 |
| Fig 5 | Enlargement of Symbol Outline to Accommodate Application Information | 23 |
| Fig 6 | Logic Symbol Orientation Examples for Diagrams that Permit Two Orientations of Text | 24 |
| Fig 7 | Orientation of Qualifying Symbols Derived from Characteristic Curves | 26 |
| Fig 8 | Application Information: Typical Examples | 28 |
| Fig 9 | Multiple-Function Terminal (Terminal 1) Shown as Separate Lines | 29 |
| Fig 10 | Multiple-Function Terminal (Terminal 1) Shown as a Single Line | 29 |
| Fig 11 | Multiple-Function Terminal (Terminal 1) Repeated on Symbol Outline | 30 |
| Fig 12 | Abbreviated Representation of Identical Inputs and Outputs | 30 |
| Fig 13 | Abbreviated Representations of Arrays of Identical Elements | 31 |
| Fig 14 | Abutment of Symbols | 32 |
| Fig 15 | Detached Representations of Devices | 32 |
| Fig 16 | Diagram Layout | 34 |
| Fig 17 | Junctions and Crossovers | 35 |
| Fig 18 | Layout Techniques | 35 |
| Fig 19 | Grouping of Lines | 36 |
| Fig 20 | Examples of Signal Name Allocation | 39 |
| Fig 21 | Clock and Timing Pulses | 43 |
| Fig 22 | Typical Table Indicating Omitted and Highest Numerical Reference Designations | 46 |
| Fig 23 | Stylized Waveforms | 48 |
| Fig 24 | Typical Waveforms for Signal Lines | 49 |
| Fig 25 | Simplified Waveform Notations | 49 |
| Fig 26 | Repeated Symbol Simplification | 51 |
| Fig 27 | Typical Diagram Sheet with Repeated Circuit Pattern | 52 |
| Fig 28 | Single Line Representation of Connections that Are Paired with Ground | 54 |
| Fig 29 | Example of Circuit Layout Condensation | 56 |
| Fig 30 | Basic Logic Diagram for a Timing-Pulse Generator | 59 |
| Fig 31 | Detailed Logic Diagram — Using the Positive Logic Convention | 60 |
| Fig 32 | Detailed Logic Diagram — Using Direct Polarity Indication | 62 |
| Fig 33 | Typical Circuit Diagram (Direct Polarity Indication) | 64 |
| Fig 34 | Typical Circuit Diagram (Positive Logic Convention) | 66 |

TABLES

| | | |
|---------|--|----|
| Table 1 | Relationships Among States and Signal Names (Single Logic Convention) | 40 |
| Table 2 | Relationships Among States, Levels, and Signal Names (Direct Polarity Indication) | 44 |

APPENDIXES

PAGE

| | | |
|------------|---|----|
| Appendix A | Mnemonics for Signal Names | 68 |
| Appendix B | Lines and Lettering — Size and Spacing | 73 |
| | B1. Introduction | 73 |
| | B2. Basic Dimensional Relationships | 73 |
| | B3. Planning Documents for Multiple Use | 77 |
| Appendix C | Single Orientation of Lettering | 81 |

APPENDIX FIGURES

| | | |
|--------|--|----|
| Fig B1 | Minimum Spacing Between Parallel Lines | 74 |
| Fig B2 | Lettering Size | 74 |
| Fig B3 | Spacing for Lines Surrounding Lettering | 74 |
| Fig B4 | Image Area On an Original Document | 78 |
| Fig C1 | Logic Symbol Orientation Examples for Diagrams that Permit Only One Orientation of Text | 82 |

APPENDIX TABLES

| | | |
|----------|--|----|
| Table A1 | Signal Names — Alphabetically by Mnemonic | 69 |
| Table A2 | Signal Names — Alphabetically by Meaning | 71 |
| Table B1 | Basic Dimensional Relationships | 73 |
| Table B2 | Minimum Dimensions | 75 |
| Table B3 | Dimensions with Convenient Units for Lettering Height (H_c) | 76 |
| Table B4 | Dimensions with Convenient Units for Lettering Thickness (T_c) | 77 |
| Table B5 | Determining Image Areas and Reduction Ratios | 78 |
| Table B6 | Multiple-Use Examples Showing Original Lettering Thickness (T_c) | 79 |
| Table B7 | Multiple-Use Examples Showing Original Lettering Height (H_c) | 79 |